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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,768	07/24/2001	James Shutt	CYPR-CD00200	5143

7590 06/22/2004

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	5

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,768	SHUTT, JAMES	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawing (Fig. 3). The informal drawing filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawing. In unusual circumstances, the formal drawing from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Specification

3. The abstract of the disclosure is objected to because it contains more than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 9-14 and 19-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Nolan et al (US Patent no 6,052,035).

6. As per claim 9, Nolan et al teach

a bus [use of a bus in a computer system is inherent and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a processor coupled to said bus [a processor coupled to a bus is inherent in a computer system and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a memory unit coupled to said bus [a memory unit coupled to a bus is inherent to a compute system and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a plurality of input/output pins [a processor or a memory unit in a computer system having input/output pins is inherent and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system]; and

a time circuit coupled to said bus for performing a timing function, said timer circuit comprising a relaxation oscillator circuit having a first power mode and a second power mode, said first power mode and said second power mode being switchable under a control [col. 8, lines

48-63; a timing capacitor performing a timing function; first operating mode and second operating mode of the relaxation oscillator; operating mode is switchable under selection of a resistor].

7. As per claim 10, Nolan et al teach

a first current source coupled [Fig. 3; col. 3, line 14; a first current generator 200];

a second current source [Fig. 3; col. 3, line 16; a second current generator 300].

8. As per claims 11 and 20, Nolan et al teach that wherein said first current source is operable to supply a large current than said second current source [col. 8, lines 48-63].

9. As per claim 12, Nolan et al teach that wherein said first reference voltage is established across a resister [col. 8, lines 61-63].

10. As per claim 13, Nolan et al teach that wherein said second reference voltage is established across a diode-connected field effect transistor [Fig. 3; col. 3, lines 51-55].

11. As per claims 14 and 23, Nolan et al teach that the microcontroller further comprising digitally trimmable components coupled to said relaxation oscillator circuit [col. 5, lines 28-32].

12. As per claim 19, Nolan et al teach that in a relaxation oscillator circuit having a first current source for a first power mode and a second current source for a second power mode [Fig. 3; col. 8, lines 35-63], a method for generating clock signals comprising the steps of:

selecting a switch current source [col. 8, lines 56-63];

generating a reference voltage based on said switched current source [col. 8, lines 56-63]; and

in response to said reference voltage, using said relaxation oscillator circuit to generate a clock signal having an accuracy that depends on said present power mode [col. 8, lines 35-63].

13. As per claims 21 and 22, Nolan et al disclose that wherein said first power mode is a low power mode and second power mode is a very low power mode [col. 8, lines 48-60].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 15-18 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al (US Patent no 6,052,035).

16. As per claims 15 and 24, Nolan et al clearly disclose having at least three trimmable components. Nolan et al do not disclose having four trimmable components. However, a routineer in the art would understand that it is possible in a different embodiment to have more than three trimmable components. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than three trimmable components. A routineer in the art would know that a greater number of trimmable components will provide a greater accuracy of the current but at the same time increase the amount of circuitry and control logic complexity.

17. As per claims 16-17 and 25-26, Nolan et al disclose the invention substantially. Nolan et al do not expressly disclose that first current generates a current of 2 micro amps and second current source generates a current of 100 nano amps. However, Nolan et al clearly disclose that the clock frequency of the second operating mode being lower than the clock frequency of the first operating mode [col. 8, lines 56-60]. Therefore, it would have been obvious to one of

ordinary skill in the art at time the invention was made to have the first current source generating a current of 2 micro amps and second current source generating a current of 100 nano amps.

18. As per claims 18 and 27, Nolan et al disclose the invention substantially. Nolan et al do not expressly disclose that relaxation oscillator circuit generates a clock signal operating at a frequency of substantially 32 KHz. However, a routineer in the art would know that it is possible to clock the relaxation oscillator at a necessary clock according to the system requirement. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the relaxation oscillator circuit generating a clock signal operating at frequency of substantially 32 KHz.

19. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al (US Patent no 6,052,035), as applied to claim 9 above, in view of Mallard, Jr. (US Patent no 5,235,617).

20. As per claim 1, Nolan et al teach

a relaxation oscillator circuit [Fig. 3; col. 2, line 62];

a first current source [Fig. 3; col. 3, line 14; a first current generator 200];

a second current source [Fig. 3; col. 3, line 16; a second current generator 300].

Nolan et al do not disclose about a control coupled to said first current source and said second current source for switching between said first power mode and said second power mode. But, Nolan et al expressly disclose about determining the first operating mode by the selection of a resistor which is internal to the first current generator [col. 8, lines 61-63] and thus controlling the switching. However, A routineer in the art would be able to implement a control means coupled to the first current source and the second current source because it is quite well known in the art as disclosed by Mallard, Jr. [col. 15, line 67 – col. 16, line 4]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both mentioning the means of switching between two current sources wherein one teaches by having the control inside the first current source and another teaches by having a common controller to do so. Moreover, a routineer may choose one over the other as needed due to the circuitry design, spacing, complexity and condition.

21. As per claim 2, Nolan et al teach that wherein said first current source supplies a larger current than said second current source [col. 8, lines 48-63].

22. As per claim 3, Nolan et al teach that wherein said first reference voltage is established across a resister [col. 8, lines 61-63].

23. As per claim 4, Nolan et al teach that wherein said second reference voltage is established across a diode-connected field effect transistor [Fig. 3; col. 3, lines 51-55].

24. As per claim 5, Nolan et al teach that the oscillator circuit further comprising trimmable components [col. 5, lines 28-32].

25. As per claim 6, Nolan et al teach that wherein said trimmable components are digitally controlled [inherent to the system].

26. As per claims 7 and 8, Nolan et al disclose the invention substantially. Nolan et al do not expressly disclose that first current generates a current of 2 micro amps and second current source generates a current of 100 nano amps. However, Nolan et al clearly disclose that the clock frequency of the second operating mode being lower than the clock frequency of the first operating mode [col. 8, lines 56-60]. Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have the first current source generating a current of 2 micro amps and second current source generating a current of 100 nano amps.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
June 11, 2004

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